Docket No.: 0941-0932P

Application No. 10/796,965 Amendment dated January 13, 2006 Reply to Office Action of December 13, 2005

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of reducing step height, comprising:

providing a substrate comprising a low-voltage device area and high-voltage device area

divided by an isolation structure and a pad oxide layer on the surface of the low-voltage device

area and high-voltage device area;

sequentially forming a silicon nitride layer of at least about 500Å thick and a patterned

mask layer, exposing the silicon nitride layer on the high-voltage device area and parts of the

isolation structure adjacent thereto, overlying the substrate;

anisotropically etching the exposed silicon nitride layer using the mask layer as an etch

mask, exposing the high-voltage device area and parts of the isolation structure;

sequentially removing the patterned mask layer and pad oxide from the surface of the

high-voltage device area;

forming a first oxide layer on the exposed high-voltage device area and isolation structure

using the silicon nitride layer as an oxidation mask;

sequentially removing the remaining silicon nitride layer and pad oxide layer from the

surface of the low-voltage device area; and

forming a second oxide layer, thinner than the first oxide layer, on the low-voltage device

layer.

2. (Original) The method as claimed in claim 1, wherein the isolation structure comprises

a shallow trench isolation (STI) structure or field oxide (FOX) layer.

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3. (Original) The method as claimed in claim 1, wherein the first oxide is formed by thermal oxidation.

4. (Original) The method as claimed in claim 1, wherein the first oxide layer thickens gradually to a predetermined value and approximately maintains the thickness in areas further from the low-voltage device structure.

5. (Original) The method as claimed in claim 1, wherein the first oxide layer is about 1000 to 2000Å thick.

6. (Original) The method as claimed in claim 1, wherein the second oxide layer is formed by thermal oxidation.

7. (Original) The method as claimed in claim 1, wherein the second oxide layer is about 32 to 125Å thick.

8. (Original) The method as claimed in claim 1, wherein the silicon nitride layer on the low-voltage device area is removed by hot phosphoric acid.

9. (Currently Amended) A method of reducing step height, comprising:

providing a substrate having a low-voltage device area and high-voltage device area divided by an isolation structure;

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forming an patterned oxidation mask at least approximately 500Å thick-over-the-low-

voltage-device-area-and-parts of the isolation structure overlying the substrate, exposing the high-

voltage device area and parts of the isolation structure;

forming a first oxide layer on the exposed high-voltage device area and isolation structure

using the oxidation mask as a mask;

теmoving the oxidation mask; and

forming a second oxide layer, thinner than the first oxide layer, on the low-voltage device

layer.

10. (Original) The method as claimed in claim 9, wherein the isolation structure

comprises a shallow trench isolation (STI) structure or field oxide (FOX) layer.

11. (Original) The method as claimed in claim 9, wherein the oxidation mask is a silicon

nitride layer.

12. (Original) The method as claimed in claim 9, wherein the first oxidation layer is

formed by thermal oxidation.

13. (Original) The method as claimed in claim 9, wherein the first oxide layer thickens

gradually to a predetermined value and approximately maintains the thickness in areas further

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from the low-voltage device structure.

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14. (Original) The method as claimed in claim 9, wherein the first oxide layer is about 1000 to 2000Å thick.

15. (Original) The method as claimed in claim 9, wherein the second oxidation layer is

formed by thermal oxidation.

16. (Original) The method as claimed in claim 9, wherein the second oxide layer is about

32 to 125Å thick.

17. (Original) The method as claimed claim 9, wherein the oxidation mask is removed by

hot phosphoric acid.

18. (Original) The method as claimed in claim 9, further comprising a pad oxide layer on

the surface of the low-voltage device area and high-voltage device layer.

19. (Currently Amended) The-eomposite method as claimed in claim 9, further

comprising removing the pad oxide layer from the low-voltage device layer when the oxidation

mask is removed.

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